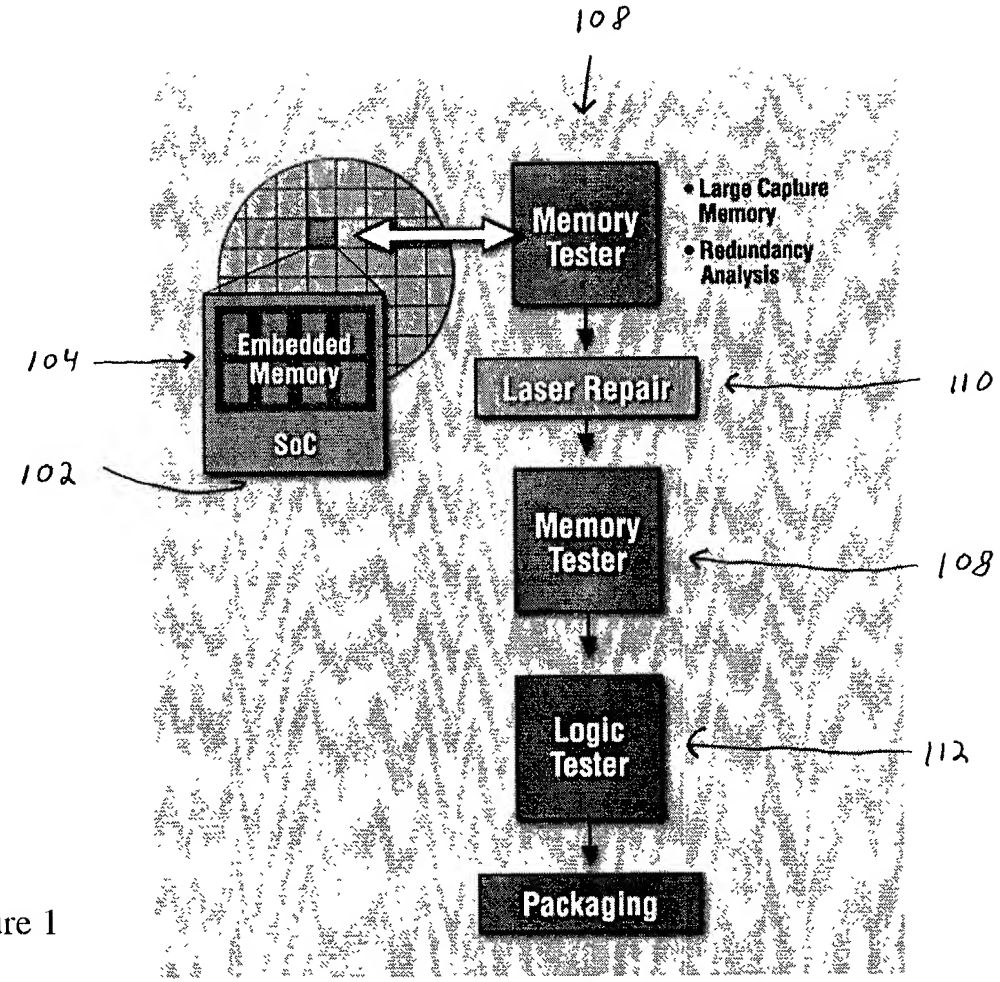

108
Memory Tester
• Large Capture Memory
• Redundancy Analysis
104
Embedded Memory
SoC
102
Laser Repair
110
Memory Tester
108
Logic Tester
112
Packaging

Figure 1

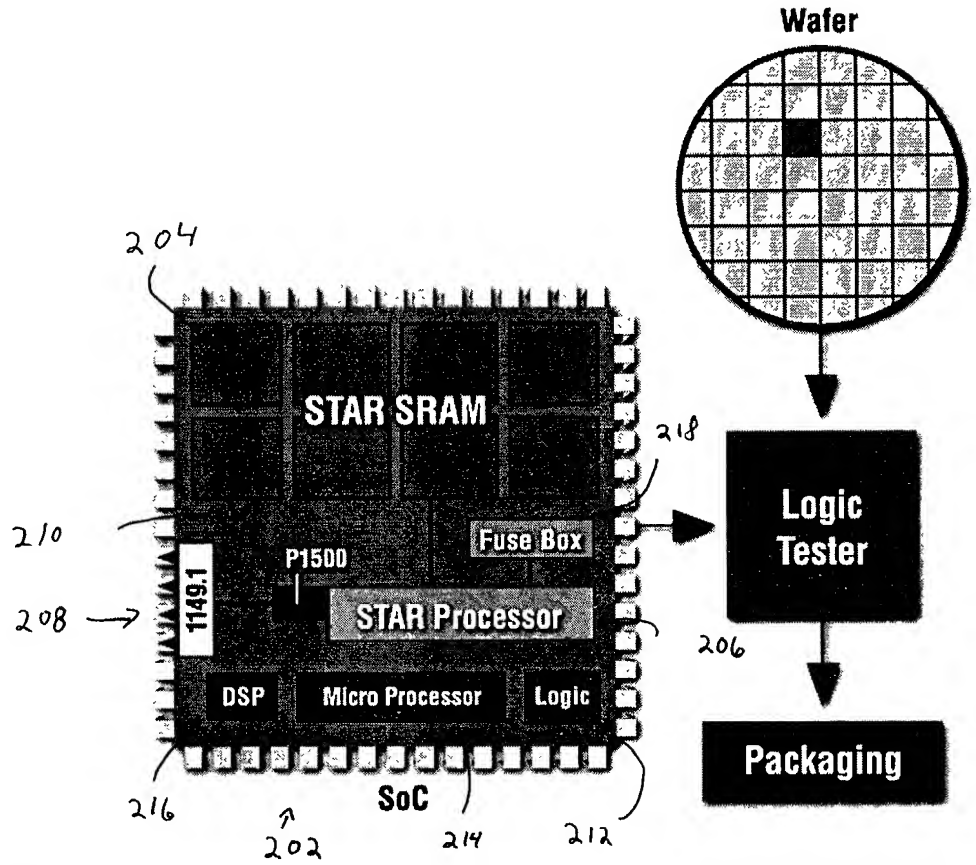


Figure 2a

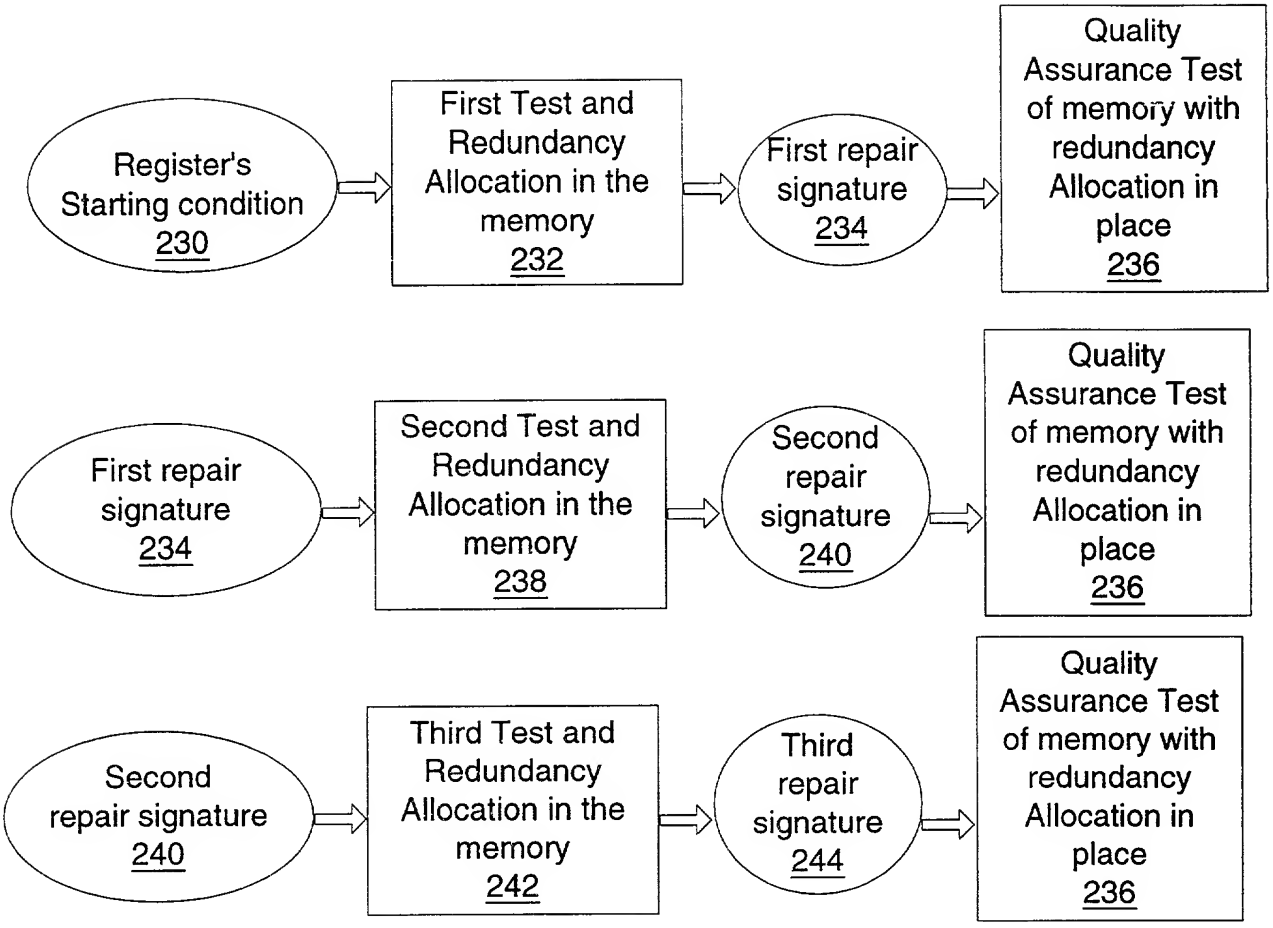


Figure 2b

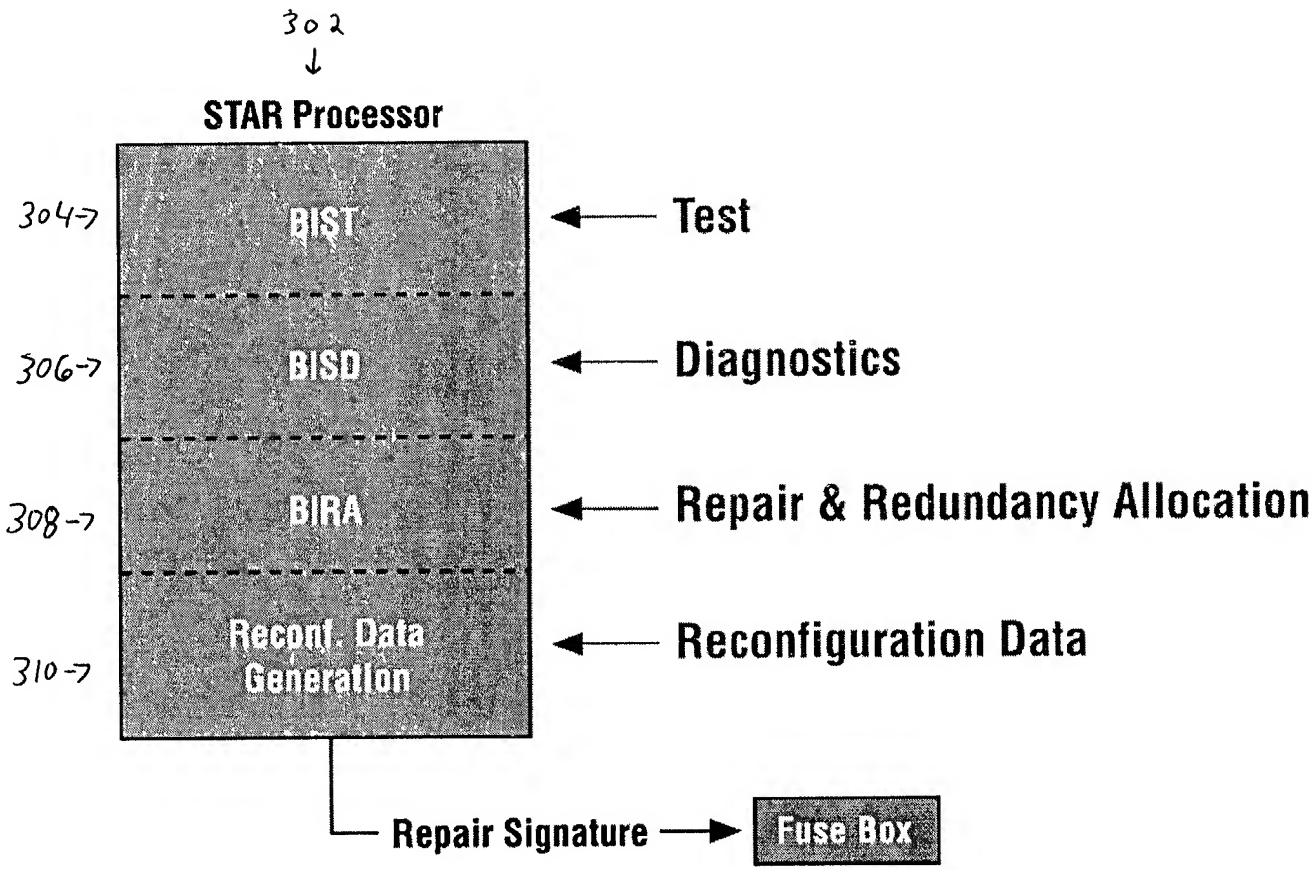

302
STAR Processor
304
BIST
Test
306
BISD
Diagnostics
308
BIRA
Repair & Redundancy Allocation
310
Reconf. Data Generation
Reconfiguration Data
Repair Signature
Fuse Box

Figure 3

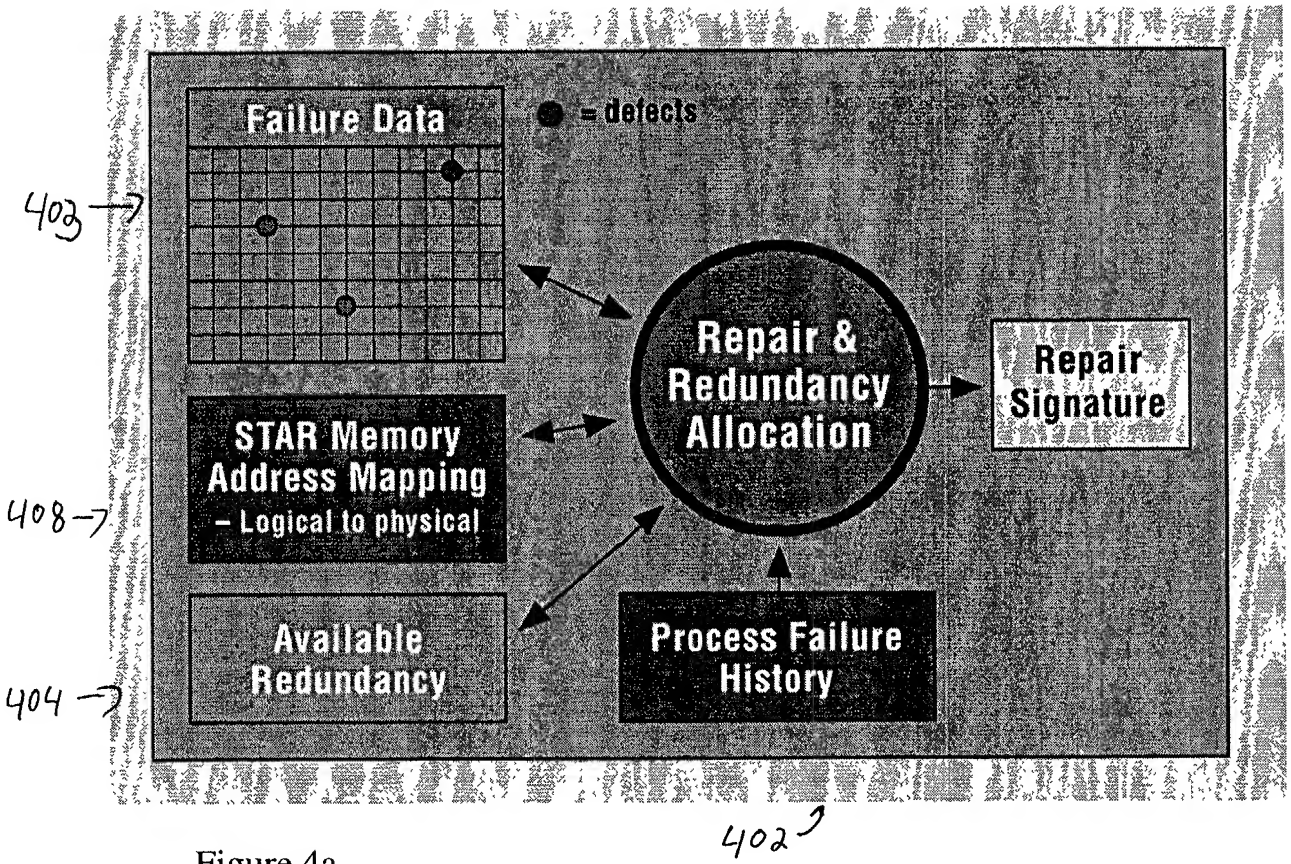

Failure Data
= defects
403
Repair & Redundancy Allocation
Repair Signature
STAR Memory Address Mapping – Logical to physical
408
Available Redundancy
404
Process Failure History
402

Figure 4a

410

0010100101000	001001000	01000	001001000	0010100101000
Upper bank Redundant column	Upper bank Redundant Row	Status Bits	Lower bank Redundant Row	Lower bank Redundant column
412	414	416	418	420

422

0010100101000	001001000	01000	001001000	0010100101000	0100
Upper bank Redundant column	Upper bank Redundant Row	Status Bits	Lower bank Redundant Row	Lower bank Redundant column	SubI/O Status Bits
					424

Figure 4b

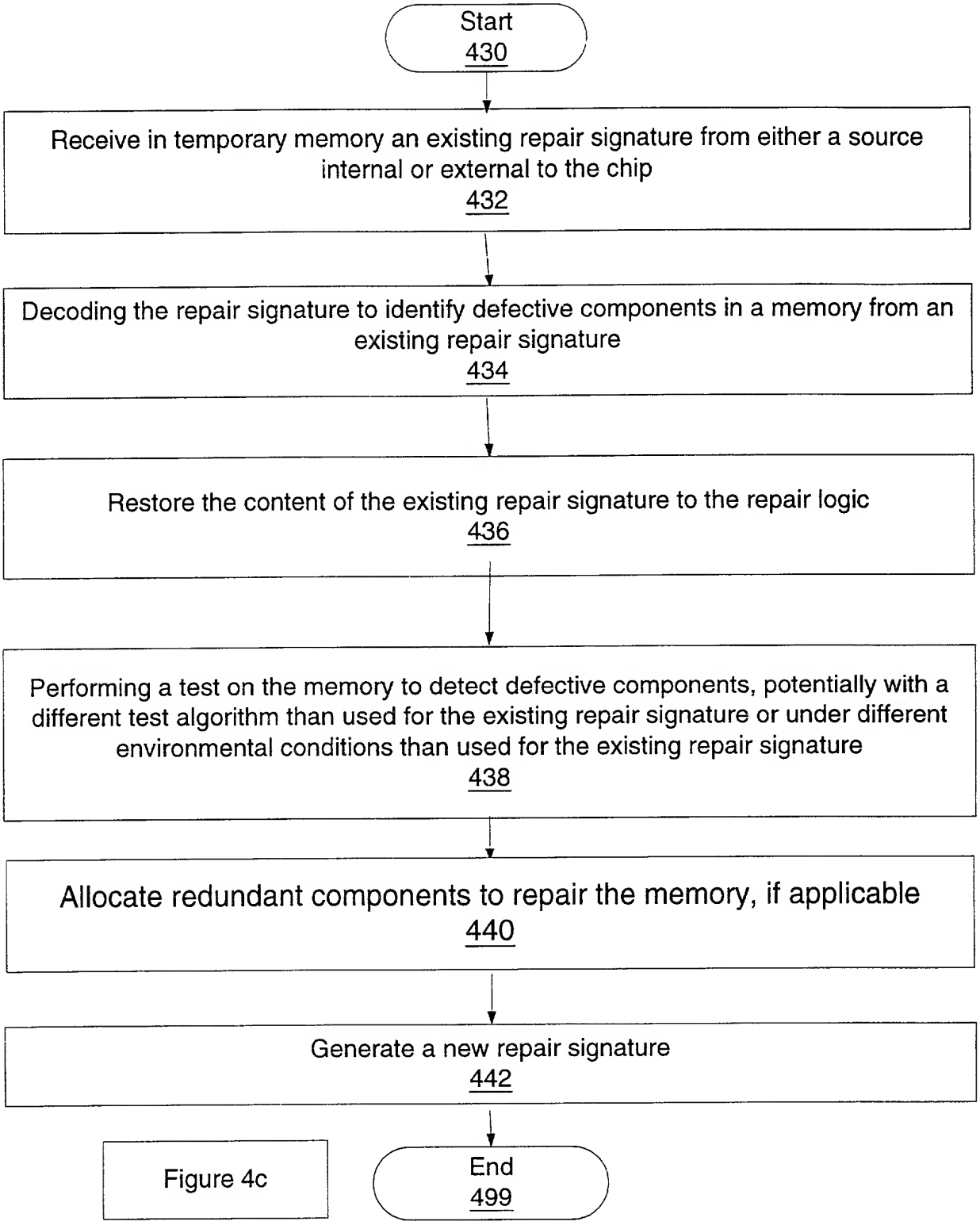


Figure 4c

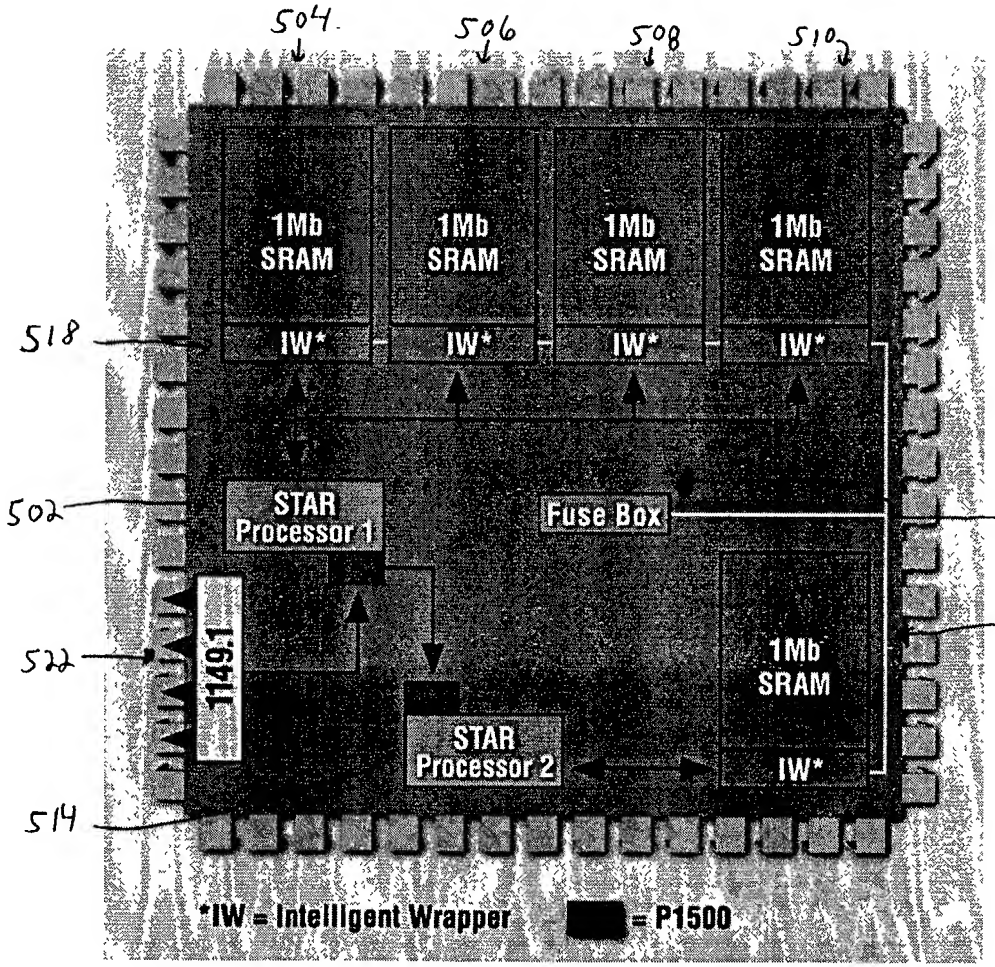


Figure 5

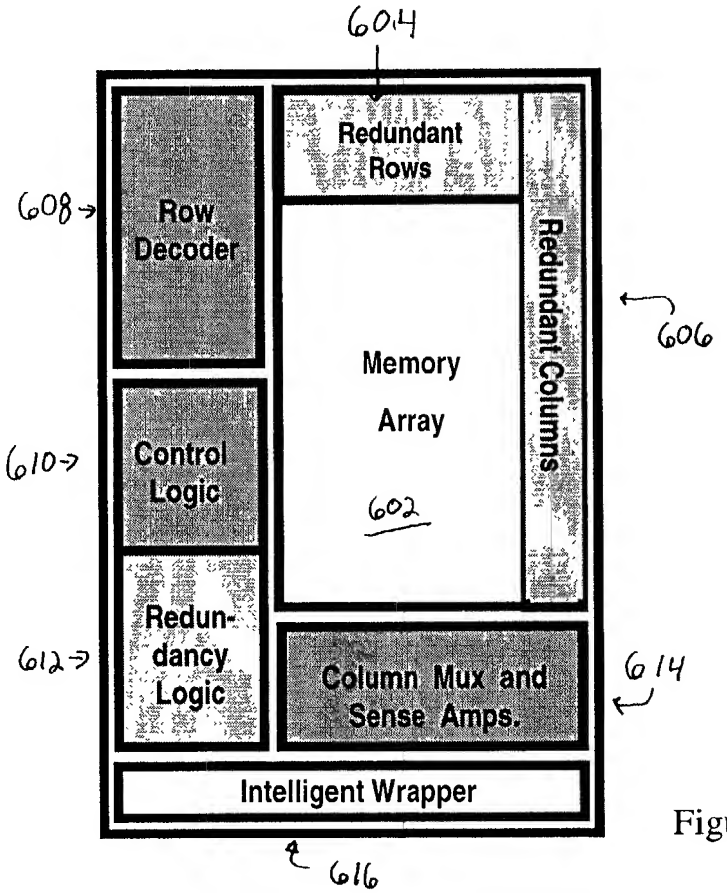


Figure 6

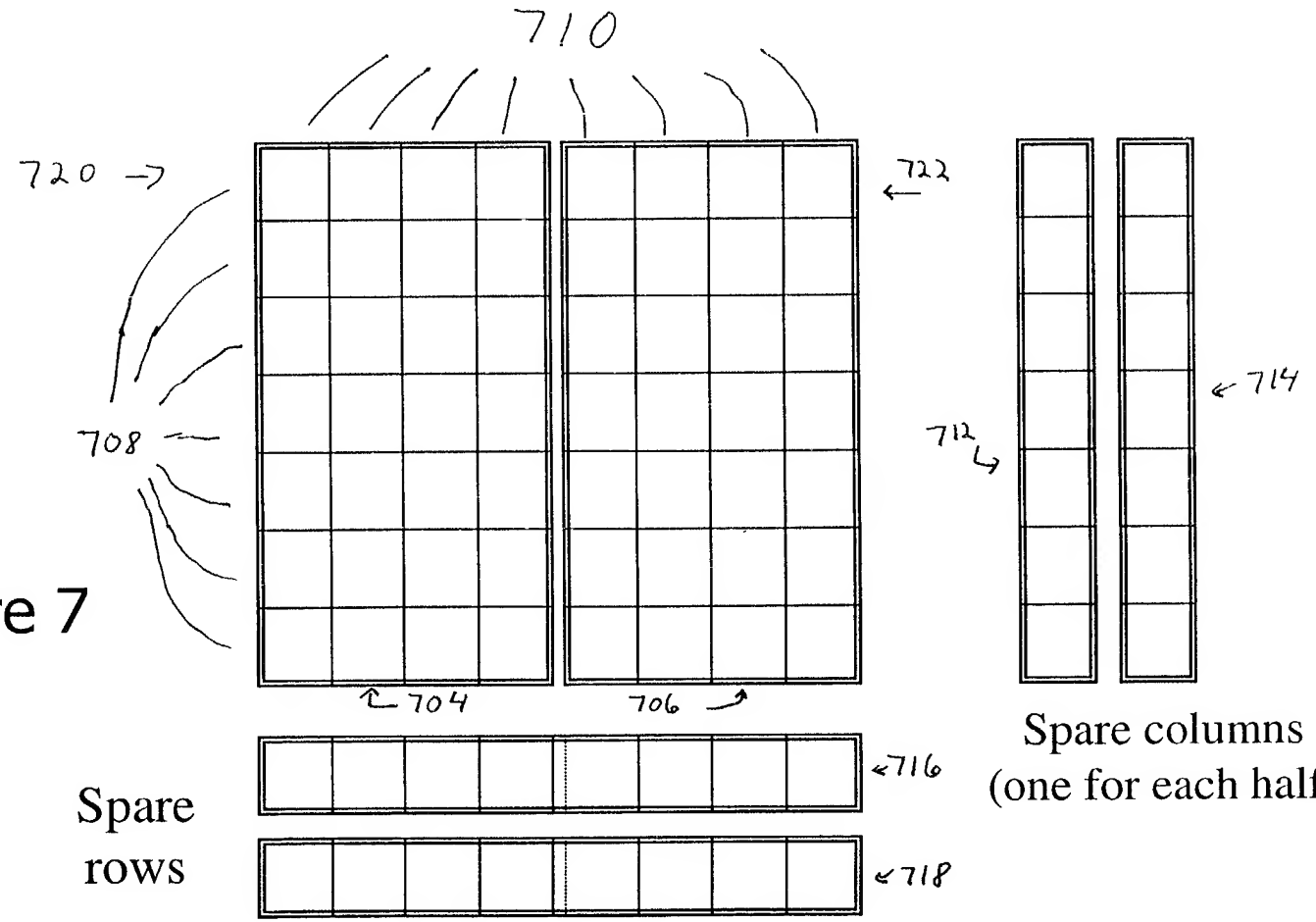

710
720
722
708
712
714
704
706
716
718
700
Spare rows
Spare columns (one for each half)

Figure 7

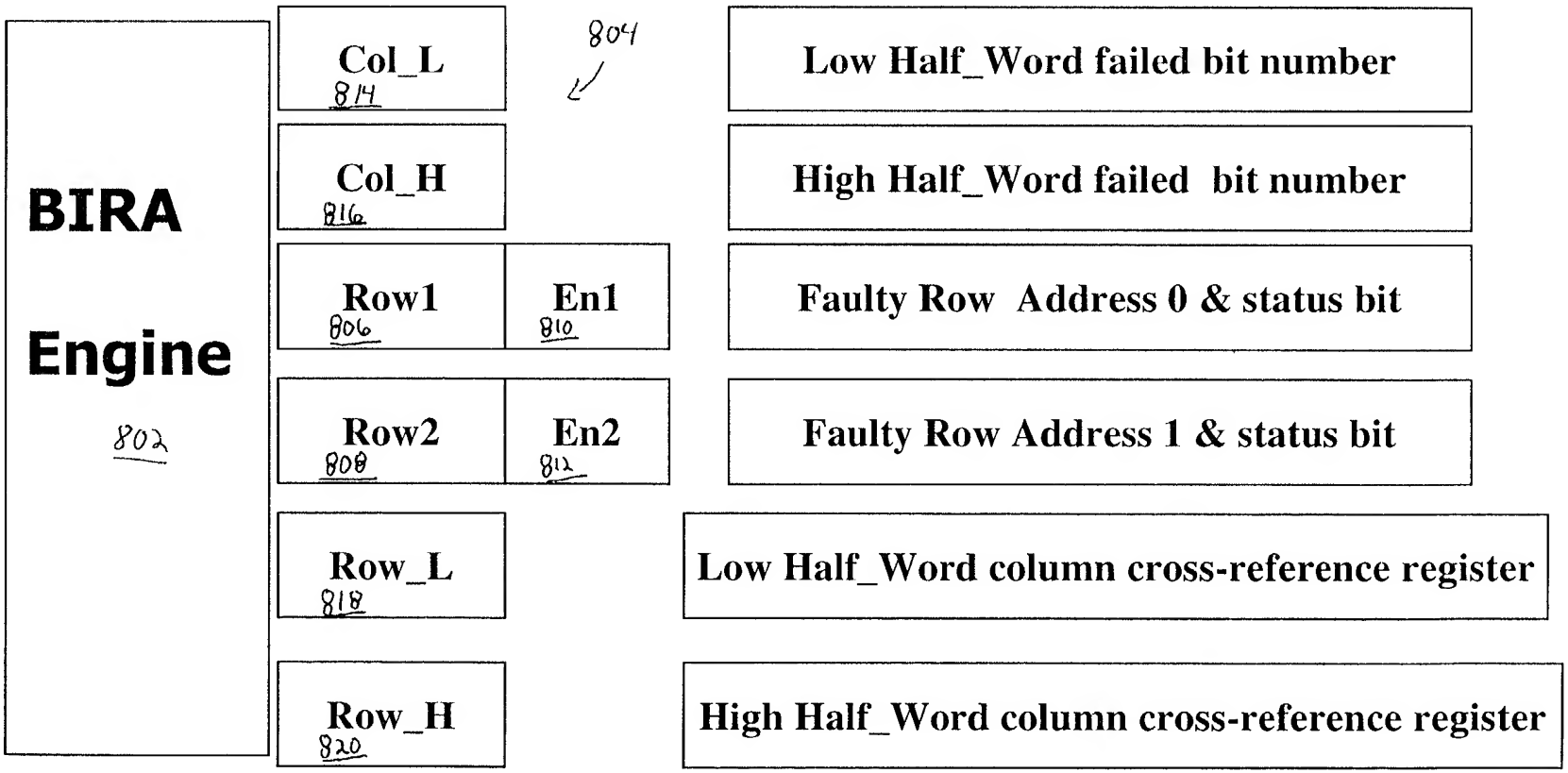

BIRA
Engine
802
Col_L
814
804
Low Half_Word failed bit number
Col_H
816
High Half_Word failed bit number
Row1
806
En1
810
Faulty Row Address 0 & status bit
Row2
808
En2
812
Faulty Row Address 1 & status bit
Row_L
818
Low Half_Word column cross-reference register
Row_H
820
High Half_Word column cross-reference register

Figure 8

Four Passes Algorithm in Order to Improve Results in the Case of Single Faults in the Row.

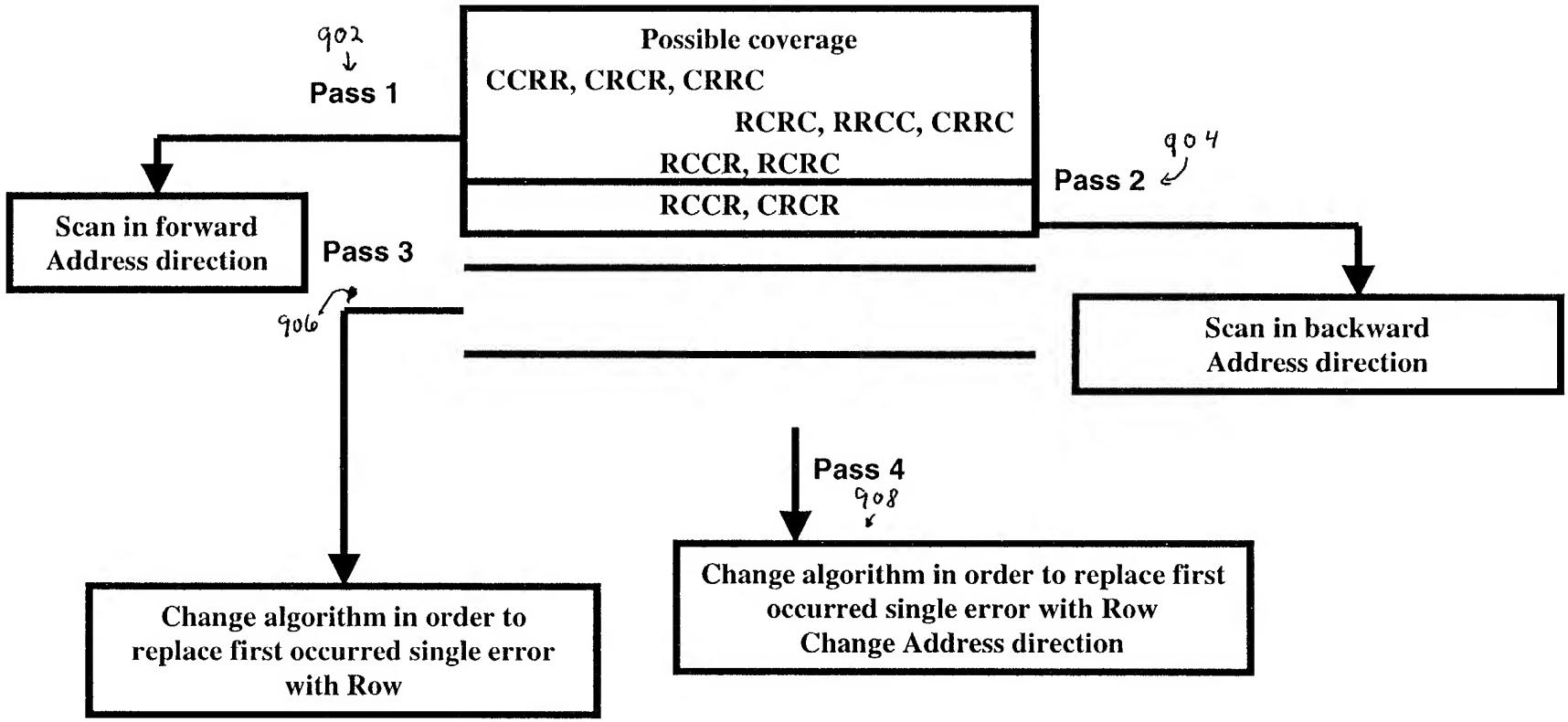
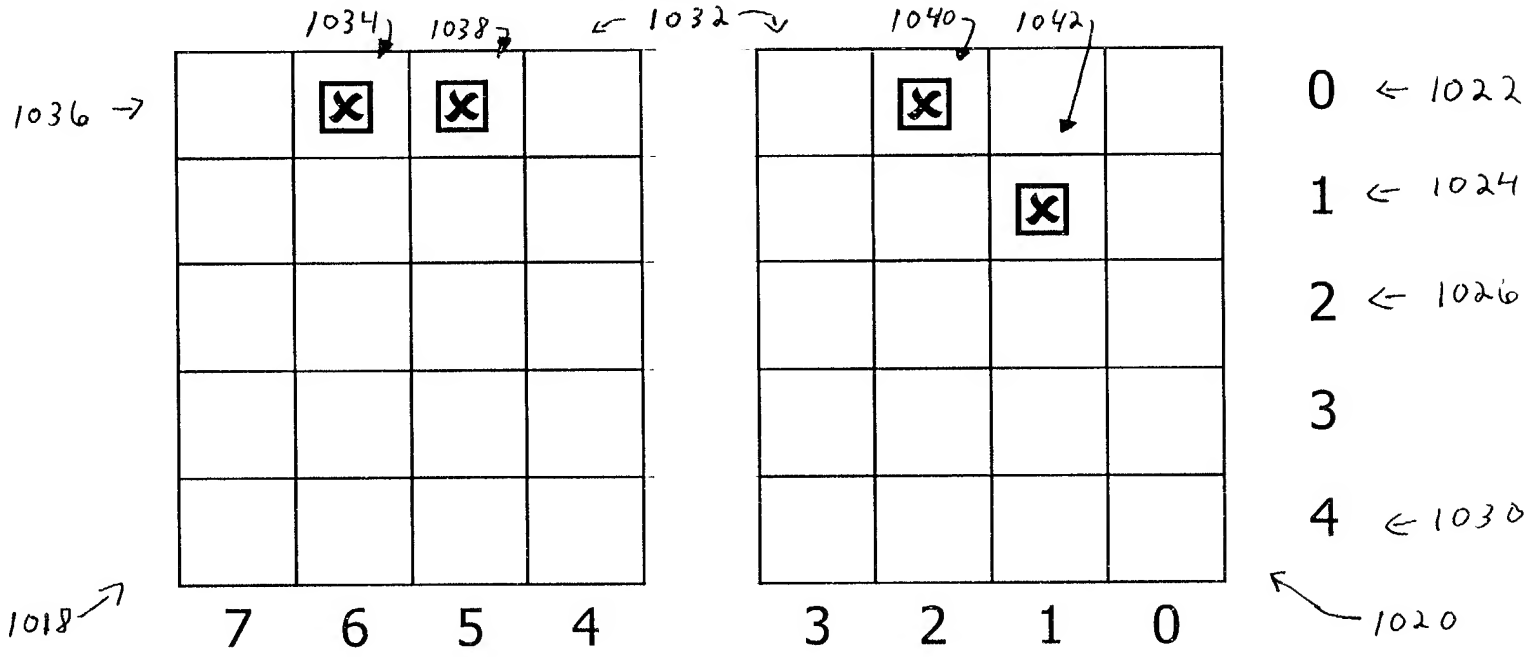


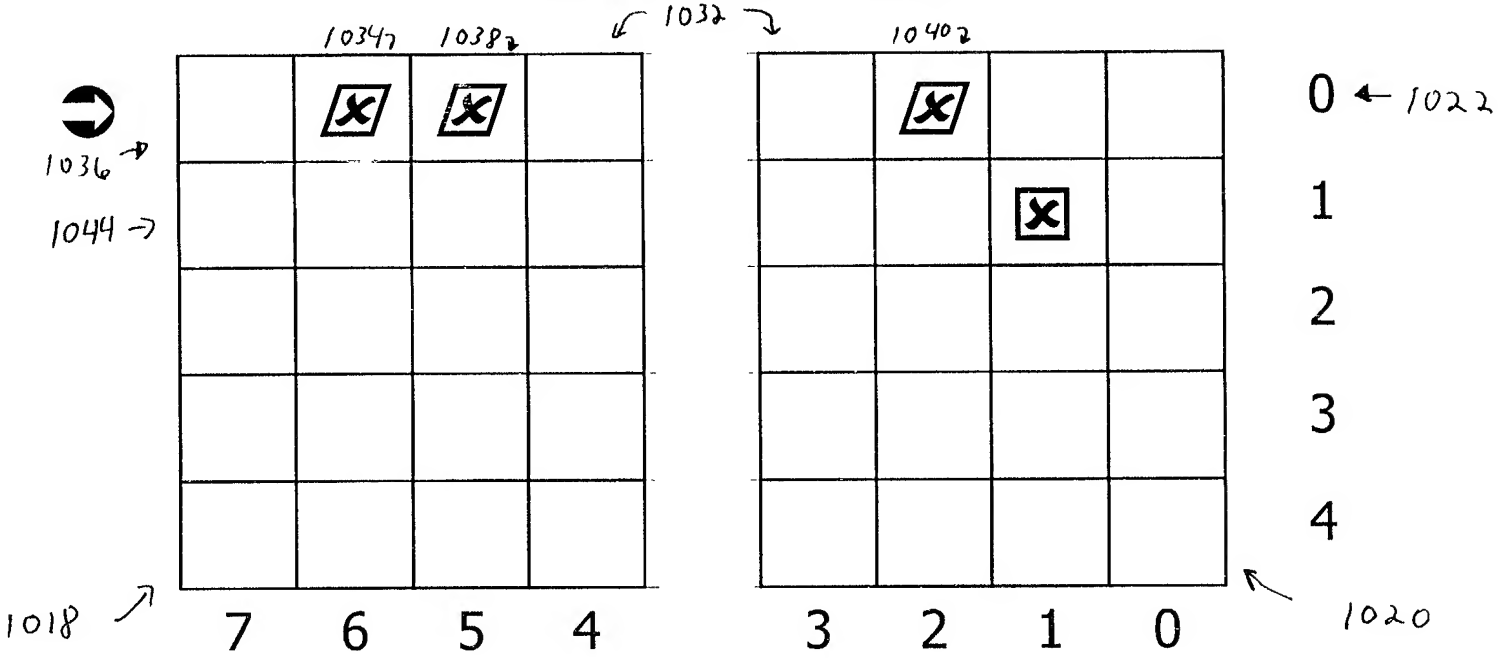
Figure 9



1004	Col_L	0	0	0	0	0	0	0	0	Col_H	1002
1008	Row_L	0				0				Row_H	1006
1012	Row 1	0				0				Row2	1010
1016	En1	0				0				En2	1014

Start condition for BIRA registers

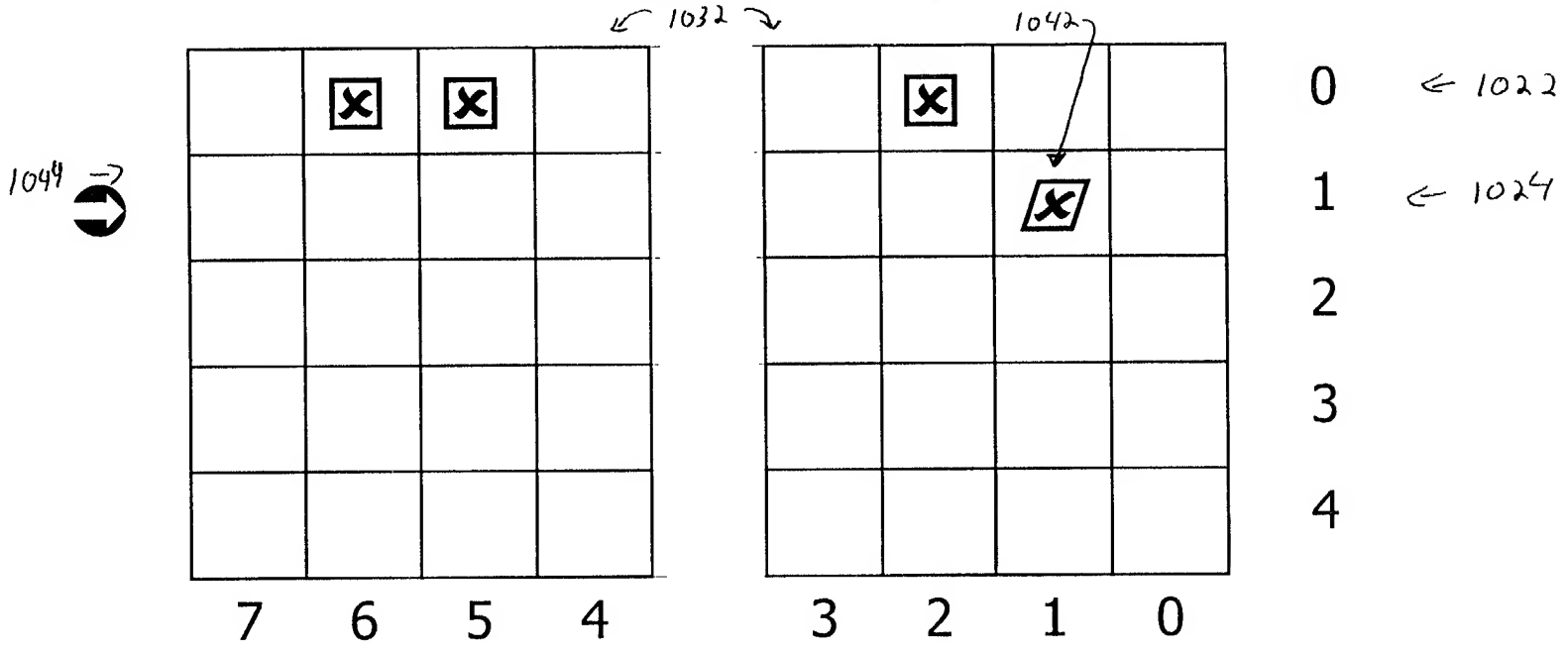
Figure 10



Col_L	0	0	0	0	0	0	0	0	Col_H
Row_L		0				0			Row_H
1012 → Row1		0				0			Row2
1016 → En1		1				0			En2

Multiple errors in Row fix with Row1

Figure 11

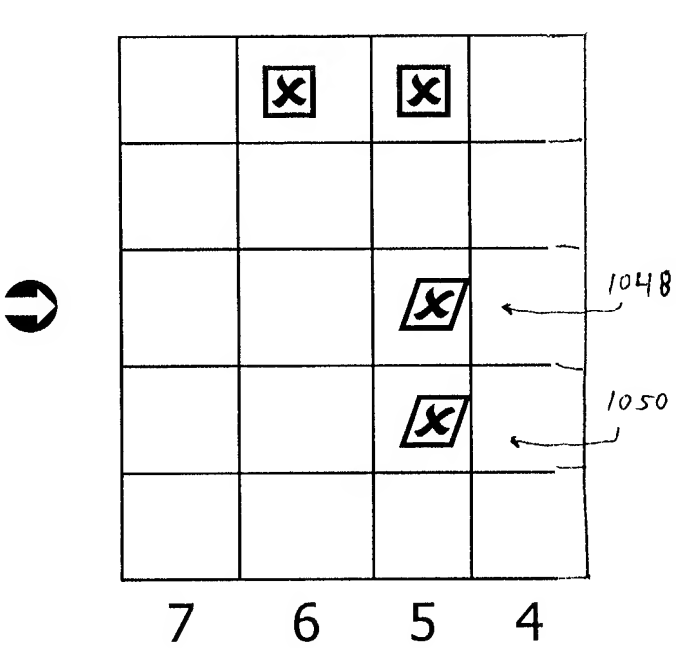


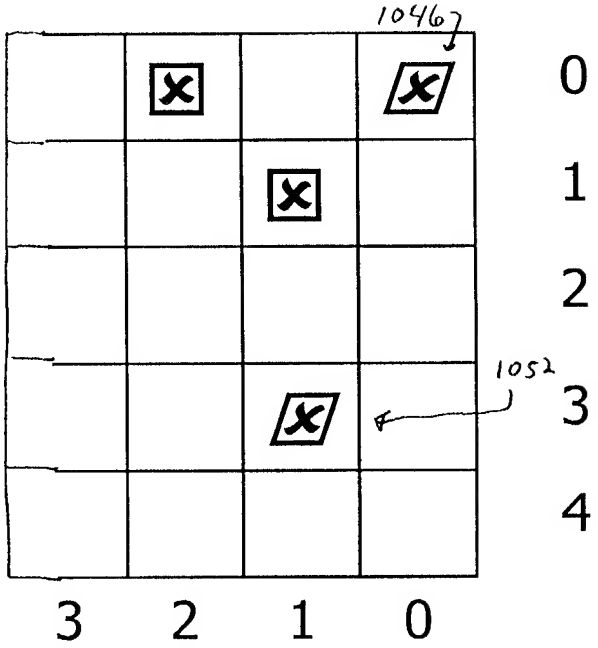
Col_L	0	0	0	0	0	0	1	0	Col_H
Row_L	0						1		Row_H
Row 1	0				0				Row2
En1	1				0				En2

1002
1006

Cover single error with column, register connectivity Row_H

Figure 12





Col_L	0	0	0	0
Row_L		0		
Row 1	0			
En1	1			

0	0	1	0	Col_H
1				Row_H
0				Row2
0				En2

1012

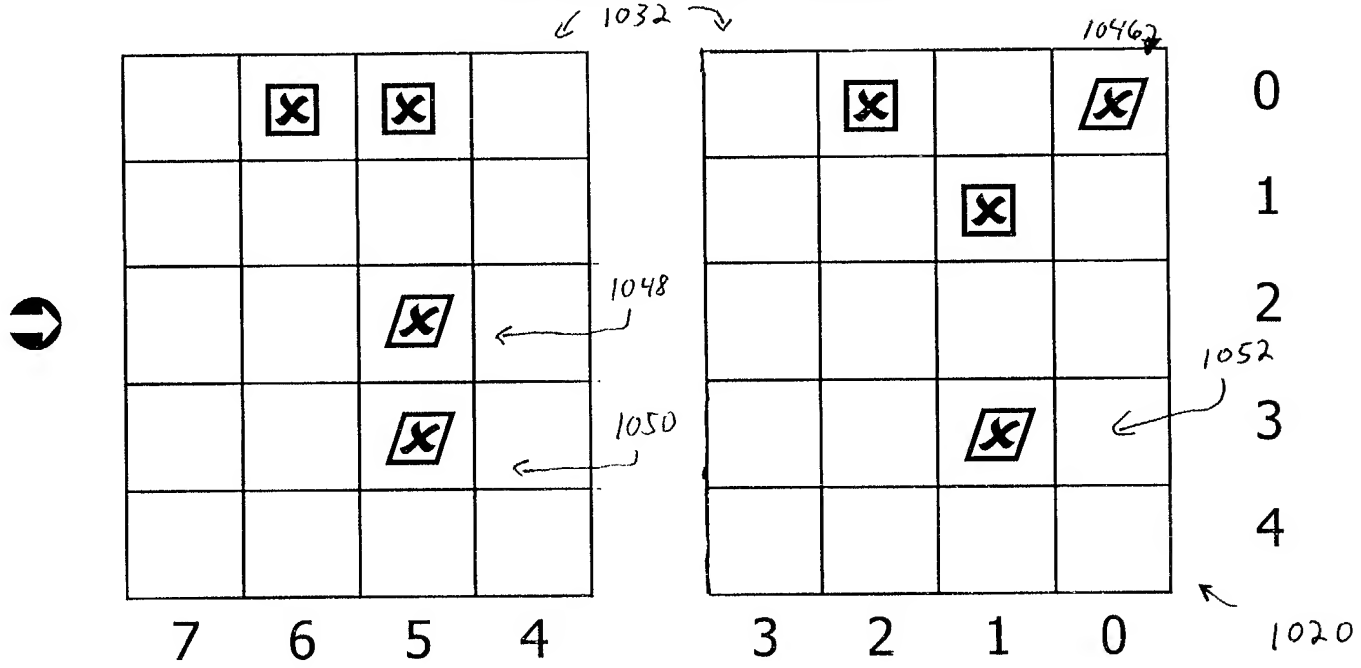
1016

1002

1006

Load content of previous signature into Registers

Figure 13



1004 →

Col_L	0	0	1	0
Row_L		2		
Row 1	0			
En1	1			

1008 →

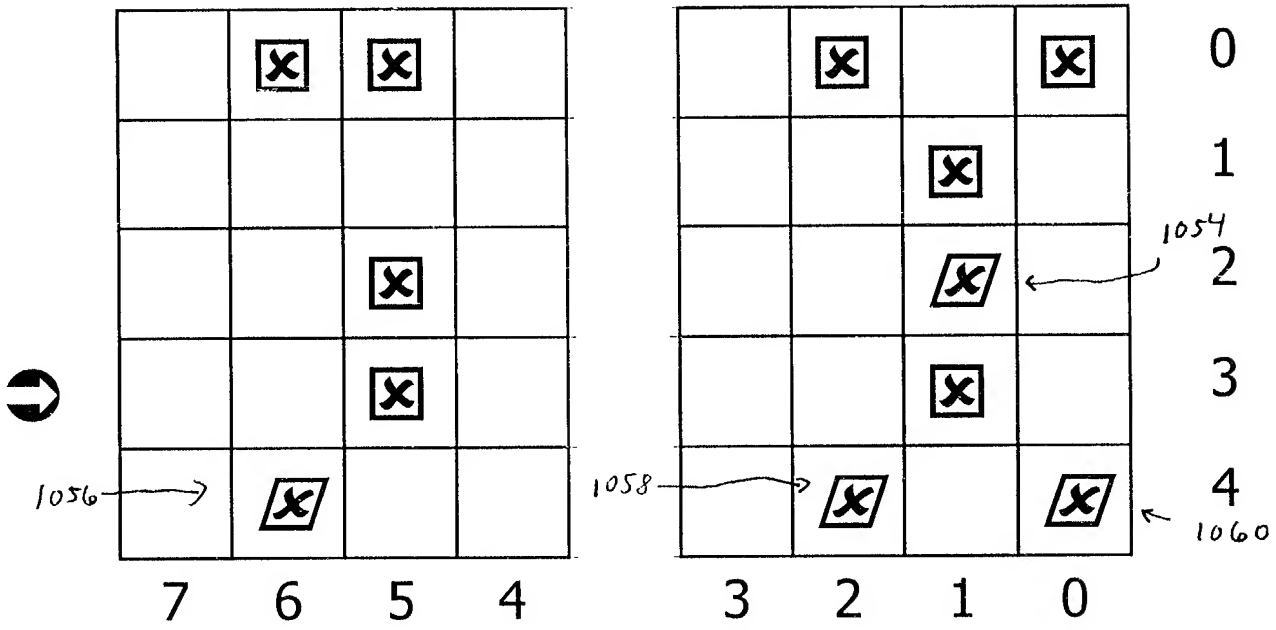
1012 →

0	0	1	0	Col_H
1				Row_H
0				Row2
0				En2

← 1002

Cover single error with column, register connectivity Row_L

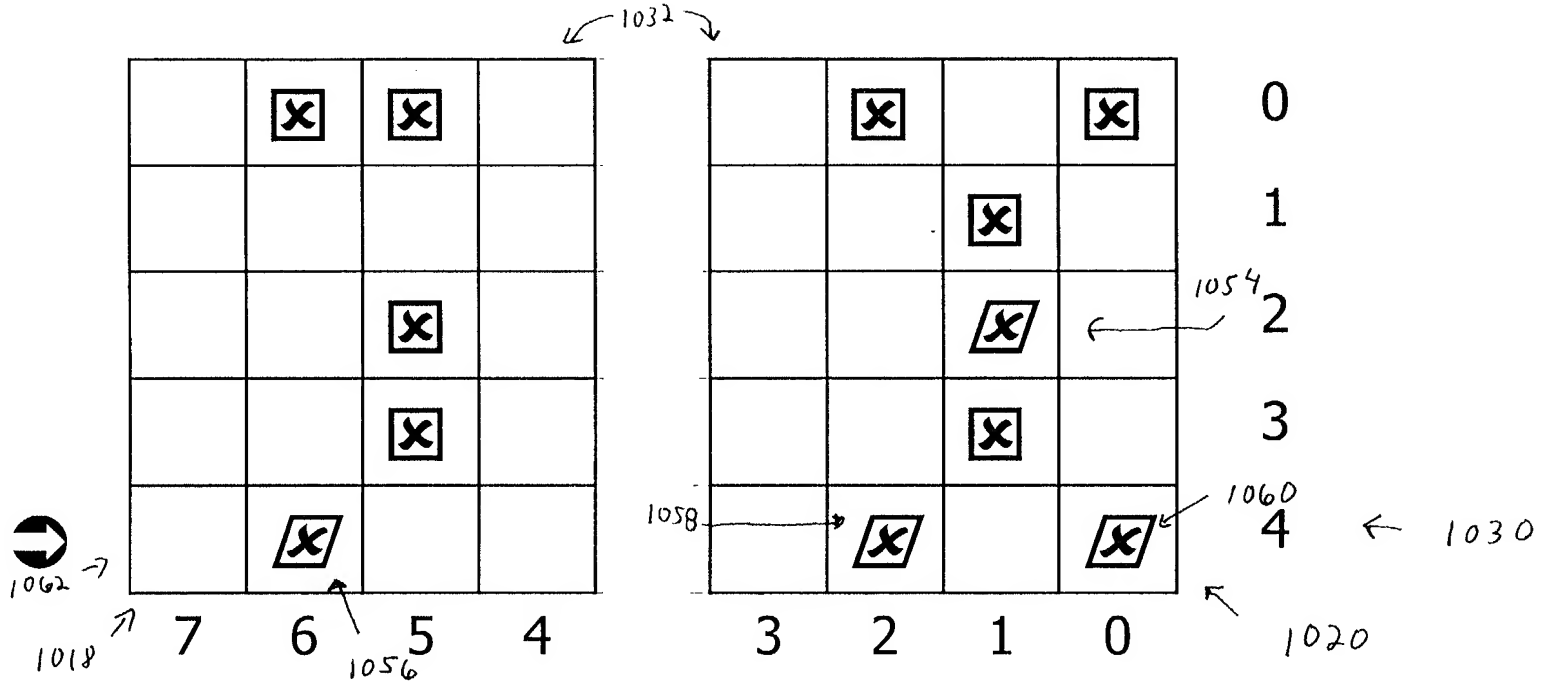
Figure 14



Col_L	0	0	1	0	0	0	1	0	Col_H
Row_ L	2				1				Row_ H
Row 1	0				0				Row 2
En1	1				1				En2

Load content of previous signature into Registers

Figure 15



Col_L	0	0	1	0	0	0	*1*	0	Col_H
Row_L	2				*1*				Row_H
Row1	0				*4*				Row2
En1	1				*1*				En2

1002
1010
1014

Multiple errors in Row fix with Row2

Figure 16